

### STS7PF30L

P-CHANNEL 30V - 0.16Ω - 7A - SO-8 STripFET™ II Power MOSFET

#### **General features**

Туре	V <sub>DSS</sub>	V <sub>DSS</sub> R <sub>DS(on)</sub>	
STS7PF30L	30V	<0.021Ω	7A

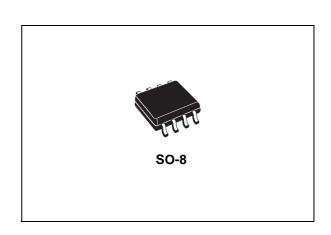
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

#### **Description**

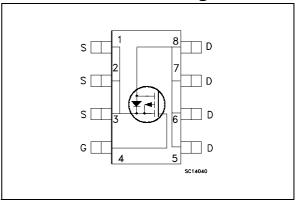
This Power MOSFET is the latest development of STMicroelectronics' unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing densisty for low on-resistance, rugged avalanche characteristics and less critical alignment steps, therefore a remarkable manufacturing reproducibility.

### **Applications**

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT.
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT



### Internal schematic diagram



#### **Order Codes**

Sales Type	Sales Type Marking		Packaging
STS7PF30L	S7PF30L	SO-8	TAPE & REEL

1 Electrical ratings STS7PF30L

# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-Source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS} = 20k\Omega$ )	30	V
V <sub>GS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	7	Α
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	4.4	Α
I <sub>DM</sub> Note 1	Drain Current (pulsed)	28	Α
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W

#### Table 2. Thermal data

Rthj-amb Note 2	Thermal Resistance Junction-ambient	50	°C/W
T <sub>j</sub>	Operating Junction Temperature	150	°C
	Storage Temperature Range	-55 to 150	°C

STS7PF30L 2 Electrical characteristics

# 2 Electrical characteristics

 $(T_J = 25 \, ^{\circ}C \, unless \, otherwise \, specified)$ 

Table 3. On/off states

Symbol	Parameter Test Conditions		Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating, $V_{DS}$ = Max Rating, $T_c$ =125°C			1 10	μΑ μΑ
I <sub>GSS</sub>	Gate Body Leakage Current (V <sub>DS</sub> = 0)	V <sub>DS</sub> = ± 16V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	1.6	2.5	V
R <sub>DS(on)</sub>	Static Drain-Source On Resistance	$V_{GS}$ = 10 V, $I_{D}$ = 3.5A $V_{GS}$ = 4.5 V, $I_{D}$ = 3.5A	0.011 0.016	0.016 0.022	0.021 0.028	Ω

Table 4. Dynamic

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> Note 3	Forward Transconductance	$V_{DS} = 20V_{,} I_{D} = 3.5A$		16		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$ , $f = 1MHz$ , $V_{GS} = 0$		2600 523 174		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> = 15V, I <sub>D</sub> = 7A, V <sub>GS</sub> = 4.5V		28 8.75 12.35	7	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on Delay Time Rise Time	$V_{DD} = 15V, I_{D} = 3.5A$ $R_{G} = 4.7\Omega, V_{GS} = 4.5V,$ (see Figure 13)		68 54		ns ns
t <sub>d(off)</sub>	Turn-off Delay Time Fall Time	$V_{DD} = 15V, I_{D} = 3.5A$ $R_{G} = 4.7\Omega, V_{GS} = 4.5V,$ (see Figure 13)		65 23		ns ns

577

2 Electrical characteristics STS7PF30L

Table 6. Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> Note 1	Source-Drain Current Source-Drain Current (pulsed)				7 28	A A
V <sub>SD</sub>	Forward On Voltage	$I_{SD} = 7A$ , $V_{GS} = 0$			1.2	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7A$ , di/dt = 100A/ $\mu$ s $V_{DD} = 15V$ , $T_j = 150$ °C (see Figure 15)		40 46 2.3		ns nC A

<sup>(1)</sup> Pulse with limited by safe operating area

Note: For the P-CHANNEL MOSFET the polarity of voltages and current have to be reversed

<sup>(2)</sup> When mounted on 1inch² FR-4 board (t  $\leq$  10 $\mu$ s)

<sup>(3)</sup> Pulsed: pulse duration = 300µs, duty cycle 1.5%

STS7PF30L 2 Electrical characteristics

## 2.1 Electrical characteristics (curves)

Figure 1. Safe Operating Area

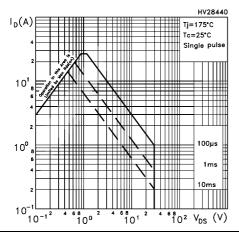


Figure 2. Thermal Impedance

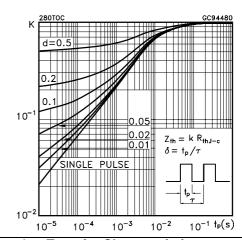
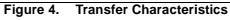
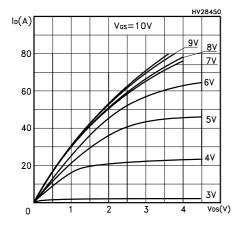


Figure 3. Output Characteristics





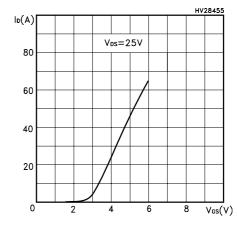
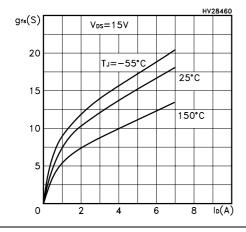
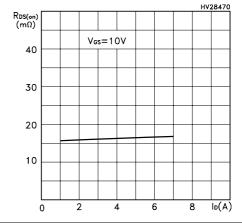


Figure 5. Transconductance

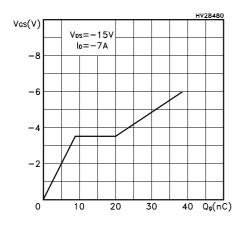
Figure 6. Static Drain-Source on Resistance





2 Electrical characteristics STS7PF30L

Figure 7. Gate Charge vs Gate-Source Voltage Figure 8. Capacitance Variations



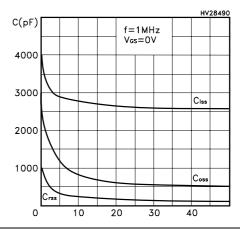
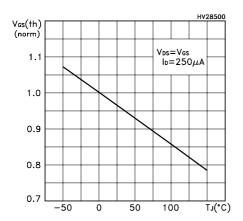


Figure 9. Normalized Gate Threshold Voltage Figure 10. Normalized on Resistance vs vs Temperature Temperature



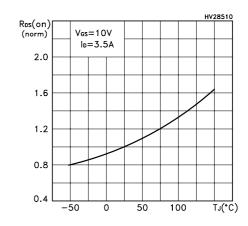


Figure 11. Source-Drain Diode Forward Characteristics

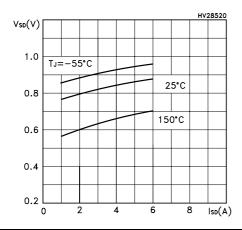
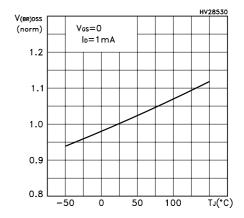


Figure 12. Normalized Breakdown Voltage vs
Temperature

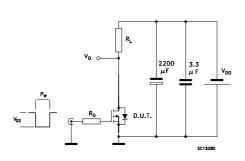


STS7PF30L 3 Test Circuits

## 3 Test Circuits

Figure 13. Switching Times Test Circuit For Resistive Load

Figure 14. Gate Charge Test Circuit



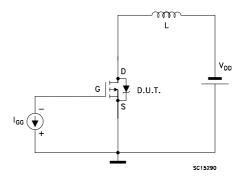
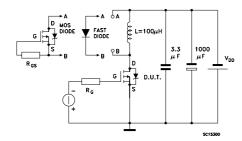


Figure 15. Test Circuit For Inductive Load Switching and Diode Recovery Times



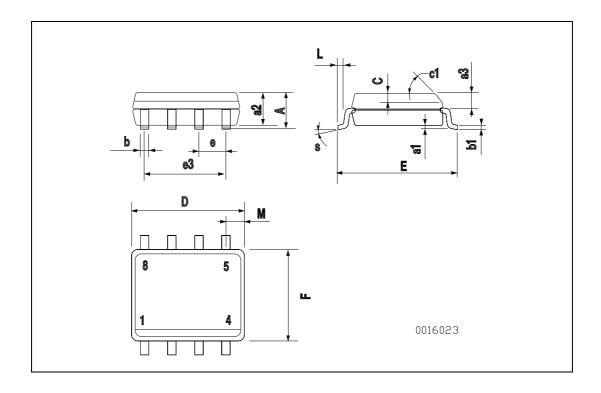
**577** 

# 4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: <a href="https://www.st.com">www.st.com</a>

#### **SO-8 MECHANICAL DATA**

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45 (	typ.)		
D	4.8		5.0	0.188		0.196
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S		•	8 (n	nax.)	•	•



**5**//

5 Revision History STS7PF30L

# **5** Revision History

Date	Revision	Changes
13-Dec-2003	1	First Issue
25-Jun-2004	2	Preliminary Data
18-Jan-2005	3	Modified value on table 5
29-Sep-2005	4	Complete version
09-Nov-2005	5	New template

STS7PF30L 5 Revision History

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